L2: Entry 2 of 10 File: USPT Jan 1, 2002

DOCUMENT-IDENTIFIER: US 6336158 B1
TITLE: Memory based I/O decode arrangement, and system and method using the same

Detailed Description Text (43):
As a final note, as the above-mentioned Low Pin Count (LPC) Interface Specification gains wide acceptance, and as ISA buses get phased out from being included in newly manufactured system, most (if not all) I/O devices (e.g., previous ISA legacy devices such as floppy disk controllers and keyboard controllers; docking station interface 115) will migrate to the LPC bus 170, e.g., a single LPC bus 170 extending from the I/O controller 108. Accordingly, it can be seen that the above-described embodiment having I/O decode information with respect to all agents/devices being provided within the I/O decode map, and having all bus transaction decoding/assertions performed by I/O controller 108, may become the most desirable arrangement within a computing system.

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L2: Entry 2 of 10 File: USPT Jan 1, 2002

US-PAT-NO: 6336158
DOCUMENT-IDENTIFIER: US 6336158 B1

TITLE: Memory based I/O decode arrangement, and system and method using the same

DATE-ISSUED: January 1, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Martwick; Andrew W.	Folsom	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 09/ 182443 [PALM]
DATE FILED: October 30, 1998

INT-CL: [07] G06 F 12/00, G06 F 13/00, G06 F 13/14, G06 F 13/12, G06 F 12/10

US-CL-ISSUED: 710/104; 710/1, 710/3, 710/9, 710/10, 710/36, 710/101, 710/103, 710/107, 710/113, 710/126, 710/128, 710/129
US-CL-CURRENT: 710/104; 710/1, 710/10, 710/107, 710/113, 710/3, 710/36, 710/9

FIELD-OF-SEARCH: 710/129, 710/128, 710/3, 710/109, 710/101, 710/103, 710/1, 710/9, 710/10, 710/36, 710/104, 710/107, 710/113, 710/126, 711/100, 709/250, 709/201, 717/11, 370/428, 345/515

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4459662	July 1984	Skelton et al.	711/100
☐	4494232	January 1985	Dambrackas et al.	370/428
☐	4787041	November 1988	Yount	701/14
☐	4802085	January 1989	Levy et al.	710/3
☐	5568621	October 1996	Wooten	
☐	5590289	December 1996	Nardone et al.	710/109
☐	5617529	April 1997	Dao	345/515

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☐	5621900	April 1997	Lane et al.	
☐	5668949	September 1997	Nardone et al.	709/201
☐	5737610	April 1998	Sandig et al.	717/11
☐	5740376	April 1998	Carson et al.	710/101
☐	5781748	July 1998	Santos et al.	710/128
☐	5790831	August 1998	Lin et al.	710/101
☐	5838932	November 1998	Alzien	710/128
☐	5857084	January 1999	Klein	710/129
☐	5864688	January 1999	Santos et al.	710/129
☐	5884027	March 1999	Garbus et al.	709/250
☐	6070207	May 2000	Bell	710/103
☐	6076128	June 2000	Kamijo et al.	710/128
☐	6078977	June 2000	Klein	710/129
☐	6098113	August 2000	Heil et al.	710/1

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
58144959	August 1983	JP	
60233751	November 1985	JP	
63067647	March 1988	JP	
01237843	September 1989	JP	
02012468	January 1990	JP	
06161880	June 1994	JP	

OTHER PUBLICATIONS

"Two Way Mapping Device", IBM Tech. Disc. Bull., Feb. 1, 1969, V. 11, No. 9, pp. 1160-1161.*
"Swing-Mode Address Decode", IBM Tech. Disc. Bull., Mar. 1, 1985, V. 27, No. 10A, pp. 5711.*
"Peripheral Component Interconnect Daughter Card Configuration", IBM Tech. Disc. Bull., Sep. 1, 1994, V. 37, No. 9, pp. 435-440.*
Panda, P.R. et al. "Exploiting Off-Chip Memory Access Modes in High-Level Synthesis", Proceedings of the 1997 IEEE/ACM International Conference on Computer-aided Design, 1997, pp. 333-340.*
Schultz, k.J. et al. "Fully Parallel Integrated CAM/RAM Using Preclassification to Enable Large Capacities", Solid-State Circuits, IEEE Journal of, vol. 31, Issue 5, May 1996, pp. 689-699.*
Wu, Y.-J. et al. "A CAM-based Decorder of Convolutionally-Encoded Data", Circuits and Systems, 1991., IEEE International Symposium on, 1991, vol. 5, pp. 2955-2958.*
Shubat, A. et al. "Mappable Peripheral Memory for High Speed Applications", CompEuro '89., `VLSI and Computer Peripherals`, Proceedings, 1989, pp. 1/56-1/58.

ART-UNIT: 2782

PRIMARY-EXAMINER: Lee; Thomas

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ASSISTANT-EXAMINER: Schuster; Katharina

ATTY-AGENT-FIRM: Antonelli, Terry, Stout & Kraus, LLP

ABSTRACT:

An input/output (I/O) decode arrangement including an I/O decode map in a form of a memory block and containing, before start of any bus I/O transactions, I/O address decode information useable for I/O address decoding for bus transaction ownership, for at least a portion of, and preferably all, possible I/O addresses in a system. Further included are: an I/O decode map pointer adapted to point to a memory address where said I/O decode map is located; an I/O decode cache adapted to cache said decode information with respect to ones of I/O addresses of which accessing has been previously performed with respect to said I/O decode map; and an I/O snooper/storer adapted to snoop said I/O decode map with any I/O address to retrieve said decode information corresponding to said I/O address, and further adapted to store retrieved said decode information into said I/O decode cache. The I/O decode map can be located within at least one of system management memory (SMM) or basic input/output system (BIOS) memory space. Implementation can further be made in a computing system and method.

23 Claims, 8 Drawing figures

L9: Entry 1 of 12 File: USPT Apr 20, 2004

DOCUMENT-IDENTIFIER: US 6725320 B1
TITLE: I2C bus switching devices interspersed between I2C devices

CLAIMS:

10. The bus as recited in claim 9, wherein the switch is a bi-directional switch capable of passing signals received at the second data connection to the first data connection and of passing signals received at the first data connection to the second data connection only when the switch is closed.

12. The bus as recited in claim 11, wherein the second switch is a bi-directional switch capable of passing signals received at the fourth data connection to the third data connection and of passing signals received at the third data connection to the fourth data connection only when the second switch is closed.

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L9: Entry 1 of 12 File: USPT Apr 20, 2004

US-PAT-NO: 6725320
DOCUMENT-IDENTIFIER: US 6725320 B1

TITLE: I2C bus switching devices interspersed between I2C devices

DATE-ISSUED: April 20, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Barenys; Michael Anton	Austin	TX		
Faust; Robert Allan	Austin	TX		
Goodwin; Joel Gerald	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 09/ 779364 [PALM]
DATE FILED: February 8, 2001

PARENT-CASE:
CROSS REFERENCE TO RELATED APPLICATIONS The present application is related to U.S. patent application Ser. No. 09/779,368 entitled "A Method for Isolating an I2C Bus Fault Using Self Bus Switching Device" filed Feb. 8, 2001 and to U.S. patent application Ser. No. 09/773,185 entitled "Dynamically Allocating I2C Addresses Using Self Bus Switching Device" filed Jan. 31, 2001. The content of the above mentioned commonly assigned, co-pending U.S. Patent applications are hereby incorporated herein by reference for all purposes.

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/316; 710/314
US-CL-CURRENT: 710/316; 710/314

FIELD-OF-SEARCH: 710/316, 710/317, 710/313, 710/124, 710/305, 710/314, 370/362, 370/463, 370/351, 709/250, 709/218, 709/253, 712/29, 712/33

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL

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☐	4016546	April 1977	Bennett et al.	
☐	5473264	December 1995	Mader et al.	
☐	5892933	April 1999	Voltz	395/311
☐	5946495	August 1999	Scholhamer et al.	395/750.01
☐	6233643	May 2001	Andrews et al.	
☐	6339806	January 2002	Foster, Sr. et al.	

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0892352	January 1999	EP	

OTHER PUBLICATIONS

International Search Report.

ART-UNIT: 2181

PRIMARY-EXAMINER: Ray; Gopal C.

ATTY-AGENT-FIRM: Yee; Duke W. McBurney; Mark E. Yociss; Lisa L. B.

ABSTRACT:

A bus switch module for use in a bus such as an I2C bus is provided. In one embodiment, the switch module includes a control unit and a switch. The control unit includes an input for receiving instructions from a bus driver as to whether to close or open the switch. The switch includes a first and a second data connection which connect the switch to a first and a second segment of the bus and includes a control input for receiving commands from the control unit. The control unit opens and closes the switch in response to instructions received from the bus driver and signals received in the first data connection are passed to the second data connection only when the switch is closed in response to a command from the control unit.

26 Claims, 4 Drawing figures

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L1: Entry 1 of 2 File: USPT Feb 4, 2003

DOCUMENT-IDENTIFIER: US 6516374 B1
TITLE: Method for docking/undocking a portable computer to/from an expansion unit

Detailed Description Text (21):
When method (2) is being used, docking/undocking is supported only when the portable computer is suspended or powered off. That is, it is impossible to support hot docking/undocking. This embodiment makes hot docking/undocking possible even for an inexpensive portable computer such as portable computer 11 having no PCI-PCI bridge chip. In the case of a portable computer provided with no PCI-PCI bridge chip, PCI bus 18 is directly connected to connector 24. Bus switch 26 is set between PCI bus 18 and connector 24.

Detailed Description Text (22):
Referring now to FIG. 5, there is depicted a flow chart of a method for hot docking portable computer 11 with expansion unit 51. First, a system is set to a Power On Suspend (POS) mode (step 111). The POS mode represents a state in which only CPU 12 and PCI bus 18 sleep. Because screen display does not disappear, a user does not sense that the system stops. To set the system to the POS mode, PCI-ISA bridge chip 25 is used. For example, PIIX4E of Intel Corporation can be used as PCI-ISA bridge chip 25. PIIX4E has a POS function for bringing the system into a suspended state as one of power management functions. Therefore, the system is set to the POS mode by using this function. When the system is set to the POS mode, it is possible to bring PCI bus 18 into an idle state (step 112). While PCI bus 18 is set to the idle state, bus switch 26 is closed to connect PCI bus 18 of portable computer 11 with PCI device 52 of expansion unit 51 (step 113).

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L1: Entry 1 of 2 File: USPT Feb 4, 2003

US-PAT-NO: 6516374
DOCUMENT-IDENTIFIER: US 6516374 B1

TITLE: Method for docking/undocking a portable computer to/from an expansion unit

DATE-ISSUED: February 4, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kinoshita; Hidenori	Machida			JP
Ogawa; Mitsuru	Yamato			JP
Kobayashi; Yasuhiro	Atsugi			JP
Katoh; Takayuki	Yokohama			JP
Miyachi; Shinobu	Sagamihara			JP
Yomo; Takashi	Fujisawa			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 09/ 548035 [PALM]
DATE FILED: April 12, 2000

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	11-105595	April 13, 1999

INT-CL: [07] G06 F 1/26, G06 F 1/18, G06 F 1/32

US-CL-ISSUED: 710/304; 710/62, 710/302, 710/303, 713/300, 713/323, 713/340
US-CL-CURRENT: 710/304; 710/302, 710/303, 710/62, 713/300, 713/323, 713/340

FIELD-OF-SEARCH: 710/62, 710/302-304, 713/300, 713/310, 713/323, 713/330, 713/340

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5488572	January 1996	Belmont	360/99.06

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☐	5860015	January 1999	Olson	713/300
☐	6209105	March 2001	Hamamoto	710/303

ART-UNIT: 2182

PRIMARY-EXAMINER: Gaffin; Jeffrey

ASSISTANT-EXAMINER: Park; Ilwoo

ATTY-AGENT-FIRM: Schelkopf; J. Bruce Bracewell & Patterson

ABSTRACT:

A method for docking/undocking a portable computer to/from an expansion unit is disclosed. The portable computer includes a main battery, and the expansion unit includes a second battery. In response to an eject event, the condition of the second battery is determined. If the second battery is in a discharging condition, a power supply route is switched from the second battery of the expansion unit to the main battery of the portable computer. If the second battery is in a charging condition, the charging condition is suspended. At this point, a hot undocking of the portable computer from the expansion unit can be performed.

2 Claims, 13 Drawing figures

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L1: Entry 2 of 2 File: USPT Mar 30, 1999

DOCUMENT-IDENTIFIER: US 5889964 A

**** See image for Certificate of Correction ****

TITLE: Method and apparatus for docking and undocking a notebook computer to and from a docking station while the notebook computer is in an active state

Brief Summary Text (12):

A method and apparatus for docking and undocking of a notebook computer to a docking station without preconditioning is described. The method of the present invention allows for quiet docking and undocking, regardless of the power mode the notebook is in. An interface within the docking station detects when the notebook computer has been inserted within the docking station, and thereby determines whether the notebook computer is in a powered on mode or a suspend mode. If the notebook is in a suspend mode, the interface powers on the notebook by asserting a resume signal. The interface then quietly docks the notebook to the docking station by enabling a switch to couple together a common system bus between the notebook computer and docking station. Events are then generated in order to cause a software routine to configure the notebook computer and docking station without prior or post user intervention.

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First Hit Fwd Refs

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L1: Entry 2 of 2 File: USPT Mar 30, 1999

DOCUMENT-IDENTIFIER: US 5889964 A

**** See image for Certificate of Correction ****

TITLE: Method and apparatus for docking and undocking a notebook computer to and from a docking station while the notebook computer is in an active state

Brief Summary Text (12):

A method and apparatus for docking and undocking of a notebook computer to a docking station without preconditioning is described. The method of the present invention allows for quiet docking and undocking, regardless of the power mode the notebook is in. An interface within the docking station detects when the notebook computer has been inserted within the docking station, and thereby determines whether the notebook computer is in a powered on mode or a suspend mode. If the notebook is in a suspend mode, the interface powers on the notebook by asserting a resume signal. The interface then quietly docks the notebook to the docking station by enabling a switch to couple together a common system bus between the notebook computer and docking station. Events are then generated in order to cause a software routine to configure the notebook computer and docking station without prior or post user intervention.

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First Hit Fwd Refs

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L1: Entry 2 of 2 File: USPT Mar 30, 1999

US-PAT-NO: 5889964
DOCUMENT-IDENTIFIER: US 5889964 A
**** See image for Certificate of Correction ****

TITLE: Method and apparatus for docking and undocking a notebook computer to and from a docking station while the notebook computer is in an active state

DATE-ISSUED: March 30, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Cho; Sung-Soo	Sunnyvale	CA		
Deng; Feng	Sunnyvale	CA		
Shah; Pranav S.	San Jose	CA		
Bryant; Diane	San Jose	CA		
Kardach; James P.	Saratoga	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 08/ 754399 [PALM]
DATE FILED: November 21, 1996

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/281; 395/283, 395/284, 395/750.03, 395/750.08
US-CL-CURRENT: 710/304; 710/104, 713/320, 713/340

FIELD-OF-SEARCH: 395/281, 395/282, 395/283, 395/500, 395/527, 395/308, 395/309, 395/284, 395/285, 395/856, 395/857, 395/858, 395/556, 395/560, 395/750.03, 395/750.08

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5463742	October 1995	Kobayashi	395/281
☐	5526493	June 1996	Shu	395/281

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☐	5596728	January 1997	Belmont	395/281
☐	5598539	January 1997	Gephardt et al.	395/281
☐	5632020	May 1997	Gephardt et al.	395/283
☐	5642517	June 1997	Shirota	395/750
☐	5668977	September 1997	Swanstrom et al.	395/500

ART-UNIT: 271

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Phan; Raymond N.

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman LLP

ABSTRACT:

Prior art quiet docking and undocking methods used an interface that was located within the notebook computer, thus adding to the complexity, weight, and power consumption of the notebook computer. The present invention provides for a method for quiet docking and undocking of a notebook computer using interface circuitry located within the docking station. Moreover, the method of the present invention provides for docking and undocking whether the notebook computer is in a powered-on or suspend mode. The notebook computer is docked and undocked to the docking station such that any transaction occurring on the system bus during the docking/undocking sequence is not affected.

12 Claims, 8 Drawing figures

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L3: Entry 1 of 2 File: USPT Feb 4, 2003

DOCUMENT-IDENTIFIER: US 6516374 B1
TITLE: Method for docking/undocking a portable computer to/from an expansion unit

Brief Summary Text (8):
An inexpensive system typically does not have a PCI-PCI bridge chip, and a PCI bus of the inexpensive system is directly connected to a PCI bus of an expansion unit by only putting a bus switch between the two buses. As a result, docking/undocking can only be executed when the system is suspended or powered off. In other words, hot docking/undocking cannot be performed.

Detailed Description Text (21):
When method (2) is being used, docking/undocking is supported only when the portable computer is suspended or powered off. That is, it is impossible to support hot docking/undocking. This embodiment makes hot docking/undocking possible even for an inexpensive portable computer such as portable computer 11 having no PCI-PCI bridge chip. In the case of a portable computer provided with no PCI-PCI bridge chip, PCI bus 18 is directly connected to connector 24. Bus switch 26 is set between PCI bus 18 and connector 24.

Detailed Description Text (22):
Referring now to FIG. 5, there is depicted a flow chart of a method for hot docking portable computer 11 with expansion unit 51. First, a system is set to a Power On Suspend (POS) mode (step 111). The POS mode represents a state in which only CPU 12 and PCI bus 18 sleep. Because screen display does not disappear, a user does not sense that the system stops. To set the system to the POS mode, PCI-ISA bridge chip 25 is used. For example, PIIX4E of Intel Corporation can be used as PCI-ISA bridge chip 25. PIIX4E has a POS function for bringing the system into a suspended state as one of power management functions. Therefore, the system is set to the POS mode by using this function. When the system is set to the POS mode, it is possible to bring PCI bus 18 into an idle state (step 112). While PCI bus 18 is set to the idle state, bus switch 26 is closed to connect PCI bus 18 of portable computer 11 with PCI device 52 of expansion unit 51 (step 113).

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L7: Entry 1 of 1 File: USPT Jan 19, 1999

DOCUMENT-IDENTIFIER: US 5862349 A
TITLE: Method and apparatus for docking and undocking a notebook computer

Detailed Description Text (6):
The common system bus is also coupled to a switch. The switch is controlled by the interface circuitry within the docking station. When the interface circuitry detects that the notebook computer has been inserted within the docking station, the switch is closed to couple the common system bus of the notebook computer with the docking station. However, because a transaction may be in progress on the common system bus, the switch is not closed until the interface circuitry determines that it is safe to do so without interrupting the transaction. The interface circuitry therefore requests control of the common system bus, and then closes the switch once control has been granted to the interface circuitry.

Detailed Description Text (7):
For one embodiment of the invention, the interface circuitry generates a docking event once the switch has been closed. The event is detected by a software routine that configures the notebook computer and docking station automatically, without prior user intervention. For instance, the software routine may load required device drivers for devices within the docking station that are coupled to the common system bus.

Detailed Description Text (36):
Note that for one embodiment, the CD1# 20b and CD2# 26b pins on the docking station side are shorter than the other pins. This is another feature that facilitates a proper generation of the connector detect event. Due to the shorter length of the CD1# 20a and CD2# 26a pins, they will only be inserted within sockets 20a and 26a once the longer pins 21b-25b have all been inserted within sockets 21a-25a. Thus, the connector detect event will be generated once all of the pins 20a-26a have been inserted within sockets 20a-26a. As an alternative embodiment wherein the docking station side comprises a socket type connection, the CD1# 20b and CD2# 26b signals on the docking station side comprise shorter sockets, rather than pins. It should be appreciated that alternate embodiments of the present invention include a connector 12 with more or less connection detect signals, comprising pins or sockets of any length relative to the other signal pins and sockets. Moreover, an alternative embodiment includes other ways of detecting insertion such as a switch which is opened and closed when the mating parts of the connector are in proper registry.